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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of: Fernando Gonzalez et al.	§	Group Art Unit: 2815
Serial No.: 10/751,141	§	Examiner: Nguyen, Joseph H.
Filed: December 31, 2003	§	
For: Transistor Having Vertical Junction Edge and Method of Manufacturing the Same	§	Atty. Docket: MICS:0114 02-1010

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January 13, 2006 — Robert A. Manware
Date

APPEAL BRIEF PURSUANT TO 37 C.F.R. §§ 41.31 AND 41.37

This Appeal Brief is being filed in furtherance to the Notice of Appeal mailed on November 14, 2005, and received by the Patent Office on November 18, 2005.

The Commissioner is authorized to charge the requisite fee of $500.00, and any additional fees which may be necessary to advance prosecution of the present application, to Account No. 13-3092, Order No. 02-1010/FLE (MICS:0114).

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1. **REAL PARTY IN INTEREST**

The real party in interest is Micron Technology, Inc., the Assignee of the above-referenced application. The Assignee of the above-referenced application will be directly affected by the Board's decision in the pending appeal.

2. **RELATED APPEALS AND INTERFERENCES**

Appellant is unaware of any other appeals or interferences related to this Appeal. The undersigned is Appellant's legal representative in this Appeal.

3. **STATUS OF CLAIMS**

Claims 12-25 are currently under final rejection and, thus, are the subject of this appeal.

4. **STATUS OF AMENDMENTS**

Appellant has not submitted any amendments subsequent to the Final Office Action mailed on July 14, 2005.

5. **SUMMARY OF CLAIMED SUBJECT MATTER**

With regard to the aspect of the invention set forth in independent claim 12, discussions of the recited features of claim 12 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a transistor (e.g., 32). *See e.g.*, Fig. 2; page 6, lines 16-19. The transistor comprises a drain terminal (e.g., 36) comprising a doped polysilicon material (e.g., 64) disposed within a first shallow cavity (e.g., 60) formed in an isolation oxide region (e.g., 58). *See e.g.*, Figs. 3-6; page 9, line 1 – page 15, line 9. The transistor further comprises a source terminal (e.g., 38) comprising a polysilicon material (e.g., 64) disposed within a second shallow cavity (e.g., 60) formed in the isolation oxide region (e.g., 58). *See e.g.*, Figs. 3-6; page 9, line 1 – page 15, line 9. The transistor further comprises a channel formed in a silicon material (e.g., 50) and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region (e.g., 68) coupled to each of the drain terminal and the source terminal. *See e.g.*, Fig. 6; page 13, line 14 – page 14, line 2. The transistor further comprises a gate (e.g., 70) disposed over the channel and comprising one or

more conductive layers disposed over a gate oxide layer (e.g., 54). *See e.g.*, Fig. 8; page 14, line 20 - page 15, line 9.

With regard to the aspect of the invention set forth in independent claim 17, discussions of the recited features of claim 17 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a memory device (e.g., 28). *See e.g.*, Fig. 2; page 6, lines 9-14. The memory device comprises a storage device (e.g., 34) and a transistor (e.g. 32). *See e.g.*, Fig. 2; page 6, lines 16-19. The transistor comprises a drain terminal (e.g., 36) comprising a doped polysilicon material (e.g., 64) disposed within a first shallow cavity (e.g., 60) formed in an isolation oxide region (e.g., 58). *See e.g.*, Figs. 3-6; page 9, line 1 – page 15, line 9. The transistor further comprises a source terminal (e.g., 38) comprising a polysilicon material (e.g., 64) disposed within a second shallow cavity (e.g., 60) formed in the isolation oxide region (e.g., 58). *See e.g.*, Figs. 3-6; page 9, line 1 – page 15, line 9. The transistor further comprises a channel formed in a silicon material (e.g., 50) and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region (e.g., 68) coupled to each of the drain terminal and the source terminal. *See e.g.*, Fig. 6; page 13, line 14 – page 14, line 2. The transistor further comprises a gate (e.g., 70) disposed over the channel and comprising one or more conductive layers disposed over a gate oxide layer (e.g., 54). *See e.g.*, Fig. 8; page 14, line 20 - page 15, line 9.

With regard to the aspect of the invention set forth in independent claim 22, discussions of the recited features of claim 22 can be found at least in the locations in the specification and drawings cited below. By way of example, an embodiment in accordance with the present invention relates to a system comprising a processor and a memory device. (e.g., 28). *See e.g.*, Fig. 2; page 6, lines 9-14; page 8, lines 1-6. The memory device comprises a storage device (e.g., 34) and a transistor (e.g. 32). *See e.g.*, Fig. 2; page 6, lines 16-19. The transistor comprises a drain terminal (e.g., 36) comprising a doped polysilicon material (e.g., 64) disposed within a first shallow cavity (e.g., 60) formed in an isolation oxide region (e.g., 58). *See e.g.*, Figs. 3-6; page 9, line 1 – page 15, line 9. The transistor further comprises a source terminal (e.g., 38) comprising a polysilicon material (e.g., 64) disposed within a second shallow cavity (e.g., 60) formed in the isolation oxide region (e.g., 58). *See e.g.*, Figs. 3-6; page 9, line 1 – page 15, line 9. The transistor further comprises a channel formed in a

silicon material (e.g., 50) and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region (e.g., 68) coupled to each of the drain terminal and the source terminal. *See e.g.*, Fig. 6; page 13, line 14 – page 14, line 2. The transistor further comprises a gate (e.g., 70) disposed over the channel and comprising one or more conductive layers disposed over a gate oxide layer (e.g., 54). *See e.g.*, Fig. 8; page 14, line 20 - page 15, line 9.

6. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

First Ground of Rejection for Review on Appeal:

Appellant respectfully urges the Board to review and reverse the Examiner's first ground of rejection in which the Examiner rejected claim 12 as being anticipated by Michejda et al. (US 2002/0190344).

Second Ground of Rejection for Review on Appeal:

Appellant respectfully urges the Board to review and reverse the Examiner's second ground of rejection in which the Examiner rejected claims 17, 18 and 22 as being unpatentable over Michejda et al. in view of Tsuchiaki (US 6,271,566).

Third Ground of Rejection for Review on Appeal:

Appellant respectfully urges the Board to review and reverse the Examiner's third ground of rejection in which the Examiner rejected claims 13-15 and 16 as being unpatentable over Michejda et al., as applied to claim 12.

Fourth Ground of Rejection for Review on Appeal:

Appellant respectfully urges the Board to review and reverse the Examiner's fourth ground of rejection in which the Examiner rejected claims 19-21 and 23-25 as being unpatentable over Michejda et al. in view of Tsuchiaki, as applied to claims 17 and 22.

7. ARGUMENT

As discussed in detail below, the Examiner has improperly rejected the pending claims. Further, the Examiner has misapplied long-standing and binding legal precedents and principles in rejecting the claims under Sections 102 and 103. Accordingly, Appellant

respectfully requests full and favorable consideration by the Board, as Appellant strongly believes that claims 12-25 are currently in condition for allowance.

A. **First Ground of Rejection:**

The Examiner rejected claim 12 under 35 U.S.C. § 102(e) as being anticipated by Michejda et al. (US 2002/0190344). Appellant respectfully traverses this rejection.

1. **Judicial precedent has clearly established a legal standard for a *prima facie* anticipation rejection.**

Anticipation under section 102 can be found only if a single reference shows exactly what is claimed. *Titanium Metals Corp. v. Banner*, 778 F.2d 775, 227 U.S.P.Q. 773 (Fed. Cir. 1985). For a prior art reference to anticipate under section 102, every element of the claimed invention must be identically shown in a single reference. *In re Bond*, 910 F.2d 831, 15 U.S.P.Q.2d 1566 (Fed. Cir. 1990). To maintain a proper rejection under section 102, a single reference must teach each and every limitation of the rejected claim. *Atlas Powder v. E.I. du Pont*, 750 F.2d 1569 (Fed. Cir. 1984). Accordingly, the Appellants need only point to a single element not found in the cited reference to demonstrate that the cited reference fails to anticipate the claimed subject matter.

2. **The Examiner's rejection of independent claim 12 is improper because the rejection fails to establish a prima facie case of anticipation.**

Independent claim 12 recites:

> A transistor comprising:
> a drain terminal comprising a doped polysilicon material disposed within a first shallow cavity formed in an isolation oxide region;
> a source terminal comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region;
> a channel formed in a silicon material and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region coupled to each of the drain terminal and the source terminal; and
> a gate disposed over the channel and comprising one or more conductive layers disposed over a gate oxide layer.

Independent claim 12 recites, *inter alia*, a transistor comprising "a drain terminal comprising a doped polysilicon material *disposed within a first shallow cavity formed in an isolation oxide region"* and "a source terminal comprising a polysilicon material *disposed within a second shallow cavity formed in the isolation oxide region.*" Emphasis added. One exemplary embodiment of the recited structure is illustrated in Figs. 3-6, which are fully described by the accompanying text in the present application. Specifically, in accordance with one exemplary embodiment, isolation oxide 58 is disposed within *trenches 52*, as illustrated in Fig. 3. Subsequently, *shallow cavities 60* are formed in the isolation oxide 58. A conductive material 64, such as polysilicon, is disposed within the cavities 60, as illustrated in Fig. 5. Finally, the structures are etched to form the source terminal 36 and the drain terminal 38 disposed within the shallow cavities 64 formed in the isolation oxide 58. As noted in the present application, the term "cavity" is often used interchangeably with the word "trench" in that they are similar structures. However, "cavity" is used in the present application to distinguish from a trench. As used in the present application, the "trench" refers to a structure formed in the substrate 50, while the "cavity" refers to structures formed in the isolation oxide 58 disposed within the trench. *See* Application, page 11, lines 16-20. As noted above, independent claim 12 recites first and second shallow cavities *formed in an isolation oxide region.*

In contrast, the Michejda reference does not disclose *shallow cavities formed in an isolation oxide region.* In stark contrast to the subject matter recited in independent claim 12 and taught by the present application, the Michejda reference discloses a semiconductor device 100 in which doped material 170 is deposited in trenches 140, 145 *formed in the semiconductor substrate.* Isolation structures 150 are formed inside the trenches 140, 145, and doped material 170 is deposited in the substrate trenches 140, 145 on top of the isolation structures 150. *See* paras. 0033-0034; *see also* Fig. 1A.

In the Final Office Action, the Examiner stated: "Michejda et al. discloses on figure 1A a transistor comprising a drain terminal 178 comprising a doped polysilicon material (para [0034], lines 5-6 and para [0058]) disposed within a first shallow cavity formed in an isolation oxide region 150 (para [0033], lines 4); a source terminal 178 comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region." Final Office Action, page 2. Thus, in the Final Office Action, the Examiner

analogized the isolation structures 150 in Michejda et al. to the isolation oxide region in claim 12. However, in the Final Office Action, the Examiner failed to identify any shallow cavities formed in the isolation structures 150 in Michejda et al. as further recited in claim 12. In the subsequent Advisory Action, the Examiner directed Appellants to the structure disclosed in Fig. 8 of Michejda. Specifically, the Examiner stated: "Michejda et al. clearly discloses in figure 8 (showing the process steps of forming the structure of figure 1A) shallow cavities 410, 415 (para [0046], line 4) formed in the isolation structure 710, 810 (para [0046], line 3 and para [0047], line 3). Note that elements 410, 415 are openings formed in the isolation structure 710, 810, and therefore considered 'shallow cavities'."

Appellants respectfully submit that the Examiner's assertions are unsupportable. That is, Michejda *does not* disclose that the trenches 410 and 415 are "formed in the isolation structure 710, 810." The Michejda reference discloses precisely *the opposite*. That is, Michejda discloses nitride sidewall spacers 710 and isolation structures 810 *formed in the trenches 410 and 415*.

Regardless of whether the Examiner is analogizing the isolation structures 150/810 (Fig. 1A/ Fig. 8) alone with the presently recited "isolation oxide regions" or analogizing the isolation structures 150/810 (Fig. 1A/ Fig. 8) in combination with the nitride sidewall spacers 165/710 (Fig. 1A/ Fig. 8) with the presently recited "isolation oxide regions," Michejda et al. in no way discloses cavities formed *in the isolation oxide regions* as recited in claim 12. As disclosed in the Michejda reference, trenches 410 and 415 are formed *in the substrate* 210, not in anything that could be fairly analogized with isolation oxide regions. *See* Fig. 4 and paragraph [0041]. After the trenches 410 and 415 are formed in the substrate 210, *nitride wall spacers 710 and isolation structures 810 are formed in the trenches 410 and 415. See* Figs. 5-8 and paragraphs [0045] – [0047]. Finally, the polysilicon 1010 is disposed over the remaining nitride wall spacers 710 and the isolation structures 810 *within the substrate trenches. See* Fig. 10 and paragraph [0049]. It is clear from the Michejda reference that the nitride wall spacers 710, isolation structures 810 and polysilicon 1010 are each disposed within the trenches 410 and 415 formed in the substrate 210.

In sharp contrast, independent claim 12 requires that the doped polysilicon material be disposed *within shallow cavities formed in the isolation oxide region.* This distinction is an important and novel element of independent claim 12. In order for the Examiner to establish a *prima facie* case of anticipation, Michejda would have to disclose shallow cavities formed in the nitride wall spacers 710 and/or the isolation structures 810. However, Michejda does not disclose such a feature. There is no cavity formed in either the spacers 710 or the isolation structures 810. The Examiner analogizes the trenches 410 and 415 with the presently recited cavities. However, the trenches 410 and 415 are *not* formed in the spacers 710 and/or isolation structures 810. Michejda teaches exactly the opposite. That is, the spacers 710 and isolation structures 810 are formed within the trenches 410 and 415. Because the trenches 410 and 415 are clearly formed *before* deposition and formation of the nitride sidewall spacers 710 and the isolation structures 810, the Examiner's position that these trenches 410 and 415 are "formed in" the sidewall spacers 710 and/or isolation structures 810 is untenable and completely contrary to the clear teachings of Michejda. There are simply no features that could conceivably be construed as trenches or cavities formed in the sidewall spacers 710 and/or the isolation structures 810. As Michejda does not disclose cavities formed in an isolation oxide region, the reference cannot possibly disclose disposing a doped polysilicon material within the cavities formed in the isolation oxide region as further recited in claim 12.

For at least the reasons set forth above, Appellants respectfully submit that claim 12 is not anticipated by the Michejda reference. Thus, the Examiner's rejection of independent claim 12 is improper. Accordingly, Appellants respectfully request that the Board overturn the Examiner's rejection and allow claim 12.

B. **Second Ground of Rejection:**

The Examiner rejected claims rejected claims 17, 18 and 22 under 35 U.S.C. § 103(a) as being unpatentable over Michejda et al. in view of Tsuchiaki (US 6,271,566). Appellant respectfully traverses this rejection.

1. **Judicial precedent has clearly established a legal standard for a *prima facie* obviousness rejection.**

The burden of establishing a *prima facie* case of obviousness falls on the Examiner. *Ex parte Wolters and Kuypers*, 214 U.S.P.Q. 735 (B.P.A.I. 1979). Obviousness cannot be established by combining the teachings of the prior art to produce the claimed invention absent some teaching or suggestion supporting the combination. *ACS Hospital Systems, Inc. v. Montefiore Hospital*, 732 F.2d 1572, 1577, 221 U.S.P.Q. 929, 933 (Fed. Cir. 1984). Accordingly, to establish a *prima facie* case, the Examiner must not only show that the combination includes all of the claimed elements, but also a convincing line of reason as to why one of ordinary skill in the art would have found the claimed invention to have been obvious in light of the teachings of the references. *Ex parte Clapp*, 227 U.S.P.Q. 972 (B.P.A.I. 1985). When prior art references require a selected combination to render obvious a subsequent invention, there must be some reason for the combination other than the hindsight gained from the invention itself, i.e., something in the prior art as a whole must suggest the desirability, and thus the obviousness, of making the combination. *Uniroyal Inc. v. Rudkin-Wiley Corp.*, 837 F.2d 1044, 5 U.S.P.Q.2d 1434 (Fed. Cir. 1988).

2. **The Examiner's rejection of independent claims 17 and 22 is improper because the rejection fails to establish a prima facie case of obviousness.**

Independent claim 17 recites:

> A memory device comprising:
> a storage device; and
> a transistor coupled to the storage device, wherein the transistor comprises:
> a drain terminal comprising a doped polysilicon material disposed within a first shallow cavity formed in an isolation oxide region;
> a source terminal comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region;
> a channel formed in a silicon material and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region coupled to each of the drain terminal and the source terminal; and
> a gate disposed over the channel and comprising one or more conductive layers disposed over a gate oxide layer.

Independent claim 22 recites:

A system comprising:
a processor; and
a memory device coupled to the processor and comprising:
a storage device; and
a transistor coupled to the storage device, wherein the transistor comprises:
a drain terminal comprising a doped polysilicon material disposed within a first shallow cavity formed in an isolation oxide region;
a source terminal comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region;
a channel formed in a silicon material and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region coupled to each of the drain terminal and the source terminal; and
a gate disposed over the channel and comprising one or more conductive layers disposed over a gate oxide layer.

Independent claims 17 and 22 each recite, *inter alia*, a transistor comprising "a drain terminal comprising a doped polysilicon material *disposed within a first shallow cavity formed in an isolation oxide region*" and "a source terminal comprising a polysilicon material *disposed within a second shallow cavity formed in the isolation oxide region.*" Emphasis added. One exemplary embodiment of the recited structure is illustrated in Figs. 3-6, which are fully described by the accompanying text in the present application. Specifically, in accordance with one exemplary embodiment, isolation oxide 58 is disposed within *trenches 52*, as illustrated in Fig. 3. Subsequently, *shallow cavities 60* are formed in the isolation oxide 58. A conductive material 64, such as polysilicon, is disposed within the cavities 60, as illustrated in Fig. 5. Finally, the structures are etched to form the source terminal 36 and the drain terminal 38 disposed within the shallow cavities 64 formed in the isolation oxide 58.

As with independent claim 12, independent claims 17 and 22 also recite first and second shallow cavities *formed in an isolation oxide region*. As discussed in detail above,

with regard to the rejection of independent claim 12, the Michejda reference does not disclose *shallow cavities formed in an isolation oxide region*. There are simply no features disclosed in Michejda that could reasonably be construed as trenches or cavities formed in the sidewall spacers 710 and/or the isolation structures 810. As Michejda does not disclose cavities formed in an isolation oxide region, the reference cannot possibly disclose disposing a doped polysilicon material within the cavities formed in the isolation oxide region as further recited in claims 17 and 22. Appellants note that the Tsuchiaki reference does not cure the deficiencies of the Michejda reference. That is, the Tsuchiaki reference does not disclose or suggest first and second shallow cavities *formed in an isolation oxide region*. Accordingly, neither of the cited references taken alone or in combination discloses or suggests each of the elements recited in claims 17 and 22.

For at least the reasons set forth above, Appellants respectfully submit that claims 17 and 22 are not rendered obvious by the Michejda reference and the Tsuchiaki reference. Thus, the Examiner's rejection of independent claims 17 and 22, as well as those claims dependent thereon, is improper. Accordingly, Appellants respectfully request that the Board overturn the Examiner's rejection and allow claims 17, 18 and 22.

C. **Ground of Rejection No. 3:**

The Examiner rejected claims 13-15 and 16 under 35 U.S.C. § 103(a) as being unpatentable over Michejda et al., as applied to claim 12. Appellants respectfully traverse this rejection.

Claims 13-15 and 16 are dependent on claim 12. As discussed at length above, the Michejda reference does not disclose or suggest each of elements recited in independent claim 12. Accordingly, the reference cannot possibly render obvious the subject matter recited in any claims dependent thereon. Therefore, Appellants respectfully request that the Board find claims 13-15 and 16 patentable over the prior art of record and reverse the Examiner's rejection of this claim for the reasons discussed above with regard to claim 12.

8. APPENDIX OF CLAIMS ON APPEAL

Listing of Claims:

12. A transistor comprising:

a drain terminal comprising a doped polysilicon material disposed within a first shallow cavity formed in an isolation oxide region;

a source terminal comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region;

a channel formed in a silicon material and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region coupled to each of the drain terminal and the source terminal; and

a gate disposed over the channel and comprising one or more conductive layers disposed over a gate oxide layer.

13. The transistor, as set forth in claim 12, wherein each of the plurality of cavities comprises a depth in the range of approximately 300 angstroms to 1500 angstroms.

14. The transistor, as set forth in claim 12, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 0.5 to 10.

15. The transistor, as set forth in claim 12, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 1 to 3.

16. The transistor, as set forth in claim 12, comprising:

a first conductive post coupled to the drain terminal and extending vertically therefrom; and

a second conductive post coupled to the source terminal and extending vertically therefrom;

wherein each of the first and second conductive posts are coupled to the respective drain and source terminals at a distance from the gate that is greater than 50% of the width of the respective drain and source terminals.

17. A memory device comprising:

a storage device; and

a transistor coupled to the storage device, wherein the transistor comprises:

a drain terminal comprising a doped polysilicon material disposed within a first shallow cavity formed in an isolation oxide region;

a source terminal comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region;

a channel formed in a silicon material and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region coupled to each of the drain terminal and the source terminal; and

a gate disposed over the channel and comprising one or more conductive layers disposed over a gate oxide layer.

18. The memory device, as set forth in claim 17, wherein the storage device comprises a capacitor.

19. The memory device, as set forth in claim 17, wherein each of the plurality of cavities comprises a depth in the range of approximately 300 angstroms to 1500 angstroms.

20. The memory device, as set forth in claim 17, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 0.5 to 10.

21. The memory device, as set forth in claim 17, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 1 to 3.

22. A system comprising:

a processor; and

a memory device coupled to the processor and comprising:

a storage device; and

a transistor coupled to the storage device, wherein the transistor comprises:

a drain terminal comprising a doped polysilicon material disposed within a first shallow cavity formed in an isolation oxide region;

a source terminal comprising a polysilicon material disposed within a second shallow cavity formed in the isolation oxide region;

a channel formed in a silicon material and arranged between each of the first shallow cavity and the second shallow cavity, wherein the channel comprises a respective doped region coupled to each of the drain terminal and the source terminal; and

a gate disposed over the channel and comprising one or more conductive layers disposed over a gate oxide layer.

23. The system, as set forth in claim 22, wherein each of the plurality of cavities comprises a depth in the range of approximately 300 angstroms to 1500 angstroms.

24. The system, as set forth in claim 22, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 0.5 to 10.

25. The device, as set forth in claim 22, wherein each of the plurality of cavities comprises an aspect ratio of less than or equal to approximately 1 to 3.

9. EVIDENCE APPENDIX

None

10. RELATED PROCEEDING APPENDIX

None